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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,979	01/17/2002	Yoshiaki Toyota	ASA-1050	5404

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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,979	TOYOTA ET AL.	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *14 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-16 and 18* is/are allowed.

6)☒ Claim(s) *1-10 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Amendment filed November 14, 2005.

Accordingly, claim 1 was amended. Currently, claims 1-18 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USPN 5,814,529) in view of Yamaji et al. (Yamaji, USPN 5,721,601).

Re claim 1, as shown in Figs. 1A-1E, Zhang discloses an image display having a plurality of thin film transistors and a plurality of capacitors on a substrate 101, wherein

a plurality of gate-lines 105 and a plurality of signal-lines 118 which cross said plurality of gate-lines in a matrix shape are formed on said substrate,

each of said thin film transistors has: an island-shaped semiconductor layer 103 having a source region, a drain region, and a channel region sandwiched between them (Fig. 1A); a first insulation film 104 formed between said island-shaped semiconductor

layer and a gate electrode 106 of the same layer as that of said gate-lines; an interlayer insulation film 109 formed above said island-shaped semiconductor layer; and a source electrode 116 and a drain electrode 117 which are come into contact with said source region and said drain region via an opening 110, 111 formed in said interlayer insulation film 109 and which exist in the same layer as that of the signal-lines 118 (Figs. 1C-1E), and

each of said capacitors 119 has: a storage electrode 107 of the same layer as that of said gate-lines 105; a second insulation film 108 formed on said storage electrode so as to be in contact therewith (Fig. 1B); and an electrode 115 which is formed on said second insulation film 108 so as to be in contact therewith via an opening 112 formed in said interlayer insulation film 109 and which exists in the same layer as that of said signal-lines 105 (Fig. 1E),

said first insulation film 104 being formed so as to cover said substrate 101 (Fig. 1A), and said second insulation film 108 being patterned to be in contact with an upper surface and side surfaces of said storage electrode 107 and an upper surface of said first insulation film 104, said source region and said drain region of said thin film transistor revealing a layer structure of an electrode havinq same layers as layers of said island-shaped semiconductor layer 103/said first insulation film 104/said interlaver insulation film 108/said signal line 118/116 as viewed from said substrate, said capacitor 119 revealing a layer structure of an electrode having same layers as layers of said first insulation film 104/said storaqe electrode 107/said second insulation film 108/said signal line 118/117 as viewed from said substrate 101 (col. 4, lines 5-12).

Zhang discloses an image display that is basically the same as that recited in claim 1 except for the first insulation film and the interlayer insulation film being of a same insulation material.

As shown in Fig. 6, Yamaji discloses a liquid crystal display device comprising a gate insulation film 7 (or first insulation film) formed of silicon oxide and an interlayer insulation film 15 including a silicon oxide, a silicon nitride film, a silicon nitride oxide film and a silicate glass or a multilayer structure formed by combining these films (col. 10, lines 41-52 and col. 12, lines 7-13).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the image display of Zhang of with the teaching of Yamaji by forming the interlayer insulation film being of a same insulation material as the first insulation film for improving step covering property (col. 12, lines 15-19).

Re claim 2, Zhang also discloses that by setting a suitable etching condition, a silicon nitride film can be used for the second insulating film as an etching stopper (col. 3, lines 34-40). It is ovious that the relative permittivity of said second insulation film is higher than that of said first insulation film which is made of silicon oxide (col. 3, lines 15-18), and hence an etching rate of said second insulating film is lower than of said first insulation film.

Re claim 3, as shown in Fig. 2A, Zhang discloses that an oxide film of the storage electrode can be used as a second insulation film (col. 4, lines 26-32).

Re claim 4, Zhang discloses that said second insulation layer 108 is formed in an upper portion and a side portion of said gate electrode 106 (Fig. 1B).

Re claim 10, Zhang discloses that said island-shaped semiconductor layer is an island-shaped polysilicon layer (col. 3, lines 12-28).

Re claim 17, Zhang discloses that the first insulation film 204 is formed of silicon oxide and, as shown in Fig. 2B, the insulation layer 208 is considered as an interlayer insulation film which is also made of silicon oxide (col. 4, lines 49-51 and 63-67).

Re claims 5 and 6, Yamaji discloses that the gate insulation film can be formed of a multilayer structure (laminate film) comprising a silicon oxide film, a silicon nitride film or a silicon nitride oxide (col. 10, lines 53-57). As known in the art, silicon nitride has higher dielectric constant than silicon oxide.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USPN 5,814,529) in view of Yamaji et al. (Yamaji, USPN 5,721,601) as applied to claims 1-6, 10 and 17, and further in view of Jung et al. (Jung, USPN 6,317,173 B1).

The image display of Zhang as modified in view of Yamaji includes all that is recited in claim 7 except for a parallel capacitor and relative permittivity of the insulation films.

As shown in Figs. 19 and 20, Jung discloses a liquid crystal display comprising a parallel capacitor including:

a first capacitor constructed by a polycrystalline silicon layer 200, a first insulation film 300, and a storage electrode 420; and

a second capacitor constructed by said storage electrode, a second insulation film 500 and an interlayer insulation film 700 which is formed on said storage electrode, and a pixel electrode 800 (col. 3, lines 48-59), wherein the first insulating layer 300 may

be made of SiO2 or SiNx and the second insulating layer may be made of SiO2 or SiNx (col. 6, lines 35-39 and 57-59) for obtaining a sufficient storage capacitance for the display (col. 24, lines 30-34).

As known in the art, the relative permittivity of SiNx (=7) is higher than that of SiO2 (=4). Accordingly, if the second insulation film is made of SiNx and the first insulation film is made of SiO2, the relative permittivity of the second insulation film is higher than that of the first insulation film. Also, the first insulation film and the second insulation film can be made of a same high dielectric constant material (SiNx).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD device of Zhang with the teaching of Jung by forming an additional capacitor constructed by a polycrystalline silicon layer, a first insulation film, and a storage electrode so as to obtain a sufficient storage capacitance for the display (col. 31, lines 1-13).

6. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USPN 5,814,529) in view of Yamaji et al. (Yamaji, USPN 5,721,601) as applied to claims 1-6, 10 and 17, and further in view of Hara et al. (Hara, USPN 6,046,790).

The image display of Zhang as modified in view of Yamazi includes all that is recited in claims 8 and 9 except for a frame memory.

As shown in Figs. 10-12, Hara discloses a LCD device comprising a frame memory 35 provided in a pixel and constructed by a capacitor 3 and a switch 5 formed on a substrate in order to temporarily store image data (col. 30, lines 5-9) so as to obtain a fast response speed for the display (col. 31, lines 1-13).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the image display of Zhang with the teaching of Hara by forming a frame memory constructed by a capacitor and a switch so as to obtain a fast response speed for the display (col. 31, lines 1-13).

Allowable Subject Matter

7. Claims 11-16 and 18 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claim 11, none of the prior art of record discloses, in combination with other limitations as claimed, a second insulation film formed in contact with a storage electrode, an upper surface of an interlayer insulation film, and a side surface of the opening formed in said interlayer insulation film.

The most relevant reference, USPN 5,814,529 of Zhang and USPN 6,493,046 B1 of Ueda, fail to disclose or suggest a storage capacitor comprising a second insulation film formed in contact with the storage electrode, an upper surface of the interlayer insulation film, and a side surface of the opening formed in said interlayer insulation film. The Zhang's reference only discloses a second insulation film 108 formed in contact with the storage electrode 107 as shown in Figs. 1A-1E. Meanwhile, as shown in Fig. 1, the Ueda's reference discloses a storage capacitor comprising a storage electrode 17a formed at the same layer as that of semiconductor layer 17, a dielectric layer 18a formed in contact with the storage electrode 17a, and an storage counter electrode 19a formed on the dielectric layer; however, the structure of this

storage capacitor is different from that of the present invention in which the storage electrode is formed at the same layer as that of the gate-lines and the storage electrode is formed at the same layer as that of signal-lines.

Re claim 14, none of the prior art of record discloses, in combination with other limitations as claimed, a manufacturing method of an image display comprising a step of patterning the second insulation film, and etching only said second insulation film so as to be in contact only with an upper surface and side surfaces of the storage electrode and an upper surface of the first insulation film.

The most relevant reference, USPN 5,814,529 of Zhang and USPN 6,493,046 B1 of Ueda, fails to disclose or suggest etching only the second insulation film so as to be in contact only with an upper surface and side surfaces of the storage electrode and an upper surface of the first insulation film. In fact, as shown in Fig. 1D of Zhang, the first and second insulation films 104 and 108 are both etched to form contact holes 113 and 114 (col. 3, lines 45-47).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

02/04/2006

ANDREW SCHECHTER
PRIMARY EXAMINER